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TITLE: Low voltage data output buffer

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PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 2000KR-0036198 (June 28, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2002001456 A	January 9, 2002	N/A	001	H03K 017/24

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2002001456A	N/A	2000KR-0036198	June 28, 2000

INT-CL (IPC): H03K017/24

ABSTRACTED-PUB-NO: KR2002001456A

BASIC-ABSTRACT:

NOVELTY - A low voltage data output buffer is provided to maintain a threshold voltage level of a transistor under 1.5V and less supply voltage by adding a bootstrap capacitor to a CMOS type output buffer.

DETAILED DESCRIPTION - The first input stage(100) includes the first PMOS(MP20) and the first NMOS(MN20) connected to a data input portion and a power source portion. The second input stage(102) includes the second NMOS(MN21) and the second PMOS(MP21) connected to the data input portion and a ground portion. An output stage(108) includes the third PMOS(MP23) and the third NMOS(MN23). An inverter(120) is used for inverting a signal of the data input portion. The first bootstrap capacitor(C10) is used for charging a predetermined voltage to compensate a threshold voltage of the transistors of the output stage(108). The first voltage compensation portion(104) includes the first control transistor(MN22) for applying the charged voltage of the first bootstrap capacitor(C10) to a gate of the third PMOS(MP23) or discharging the charged voltage. The second bootstrap capacitor(C11) is used for compensating a threshold voltage of the transistors of the output stage(108). The second voltage compensation portion(106) includes the second control transistor(MP22) for applying the charged voltage of the second bootstrap capacitor(C11) to a gate of the third NMOS(MN23) or discharging the charged voltage.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: LOW VOLTAGE DATA OUTPUT BUFFER

DERWENT-CLASS: U21

EPI-CODES: U21-B02B;

